Listing of Claims:

Entire set of pending claims:

203. (Canceled)

204. (New) An apparatus comprising:

a host interface in an optical drive controller, said host interface operable to be directly connected to a host computer via an IDE/ATA bus to communicate addresses, commands, and data through ATA command block register addresses, said host interface including a first buffer addressed by one said ATA command block register addresses and operable to store command packets, each of said command packets comprising multiple command bytes received through multiple writes by said host computer as part of a single command transfer and stored sequentially in said first buffer, wherein said first buffer provides a greater amount of storage than the width of said IDE/ATA bus.

205. (New) The apparatus of claim 204, wherein said host interface is further operable to provide access by a microcontroller to data stored in locations addressed by at least certain of said ATA command block register addresses, said microcontroller operable to control reading of information from optical media.

206. (New) The apparatus of claim 204, wherein said optical drive controller further comprises:

a path operable to communicate said addresses and commands from the host interface to a microcontroller, said microcontroller operable to control reading of information from optical media.

207. The apparatus of claim 206 wherein said microcontroller is also operable to cause the assertion of signals on DASP and PDIAG lines of said IDE/ATA bus.

208. The apparatus of claim 206, wherein said microcontroller is also operable to cause the assertion of signals on an HIRQ line of said IDE/ATA bus to generate interrupts on said host computer.

209. The apparatus of claim 206, wherein:

said host interface includes a status register addressed by another of said ATA command block register addresses, said status register including a BSY bit whose state indicates whether said host computer can access said ATA command block register addresses; and

said microcontroller can cause said BSY bit to be altered to a state that allows access by said host computer.

210. (New) The apparatus of claim 204, wherein said ATA command block register addresses address eight register locations.

211. (New) The apparatus of claim 204, wherein said IDE/ATA bus includes,

host address lines; and

a host chip select line whose signal identifies whether signals on the host address lines are carrying one of said ATA command block register addresses.

212. (New) The apparatus of claim 204, wherein host interface includes physical registers that are addressed by at least certain of said ATA command block register addresses.

213. (New) The apparatus of claim 204, wherein said host interface supports all of the signals required by the ATA transfer protocol.

214. (New) The apparatus of claim 204, wherein said IDE/ATA bus is at least 16 bits wide.

215. (New) The apparatus of claim 204, wherein the one of said ATA command block register addresses that can be used to address said first buffer is the address of a data port in the ATA transfer protocol.

216. (New) The apparatus of claim 204, wherein said host interface also includes a second buffer operable to store data to be transmitted to said host computer and addressed by the one of said ATA command block register addresses that can be used to address said first buffer.

217. (New) The apparatus of claim 216, wherein said second buffer is a queue or FIFO.

218. (New) The apparatus of claim 204, wherein said first buffer is a queue or FIFO.

219. (New) The apparatus of claim 204, wherein said optical drive controller further comprises:

a path operable to allow a microcontroller, which controls reading of information from optical media, to read said first buffer.

220. (New) The apparatus of claim 204, wherein said host interface includes a status register addressed by another of said ATA command block register addresses, said status register including a BSY bit.

221. (New) The apparatus of claim 220, wherein said host interface alters said BSY bit when necessary to indicate when said host computer is precluded from accessing said ATA command block register addresses.

222. (New) The apparatus of claim 220, wherein said host interface includes circuitry operable to clear the signal on an HIRQ line of said IDE/ATA bus responsive to said host computer reading said status register.

223. (New) The apparatus of claim 220, wherein said host interface includes circuitry operable to alter said BSY bit, responsive to command events initiated by the host computer, to a state that precludes said host computer from accessing said ATA command block register addresses.

224. (New) The apparatus of claim 223, wherein said optical drive controller further comprises:

a path operable to allow a microcontroller, which controls reading of information from optical media, to alter said BSY bit to a state that allows said host computer to access said ATA command block register addresses.

225. (New) The apparatus of claim 220, wherein said host interface is operable to assert signals on DASP and PDIAG lines of said IDE/ATA bus according to the ATA transfer protocol.

226. (New) The apparatus of claim 225, wherein said host interface is also operable to assert signals on an HIRQ line of said IDE/ATA bus according to the ATA transfer protocol.

227. (New) The apparatus of claim 226, wherein said host interface includes circuitry operable to carry out initial signal transitions on said DASP, PDIAG, and HIRQ lines in response to soft reset and execute drive diagnostic command events.

228. (New) The apparatus of claim 227, wherein said optical drive controller further comprises:

a path operable to allow a microcontroller, which controls reading of information from optical media, to control certain transitions of signals on said DASP, PDIAG, and HIRQ lines of said IDE/ATA bus.

229. (New) The apparatus of claim 220, wherein said host interface is also operable to assert signals on DASP and PDIAG lines of said IDE/ATA bus responsive to power on reset or execute diagnostic commands received from said host computer.

230. (New) The apparatus of claim 229, wherein said optical drive controller further comprises:

a path operable to allow a microcontroller, which controls reading of information from optical media, to cause the assertion of signals on DASP and PDIAG lines of said IDE/ATA bus.

231. (New) The apparatus of claim 204, wherein said host interface includes a drive/head register addressed by another of said ATA command block register addresses, said drive/head register including a DRV bit.

232. (New) The apparatus of claim 231, wherein said host interface uses said DRV bit to determine whether to store command information in said first buffer.

233. (New) The apparatus of claim 204, wherein said host interface is also operable to communicate control signals on at least certain control lines of said IDE/ATA bus.

234. (New) The apparatus of claim 233, wherein said control lines include HIRQ, DASP, and PDIAG.

235. (New) The apparatus of claim 204, wherein said host interface is also operable to assert signals on an HIRQ line of said IDE/ATA bus according to the ATA transfer protocol.

236. (New) The apparatus of claim 204, wherein said host interface is also operable to assert signals on an HIRQ line of said IDE/ATA bus to alert said host computer during data transfers.

237. (New) The apparatus of claim 204, wherein said host interface is also operable to assert signals on an HIRQ line of said IDE/ATA bus to allow said host computer to engage in multi-tasking.

238. (New) An apparatus comprising:

a host interface of an optical drive controller, said host interface operable to be directly connected to a host computer via an IDE/ATA bus to communicate addresses, commands, and data through ATA command block register addresses, said ATA command block register addresses belonging to a register address map specified by an IDE/ATA bus protocol, at least one of said ATA command block register addresses providing access to a multi-byte command packet buffer that can store multiple writes by the host computer of command information as part of the same command and that provides a greater amount of storage than the width of said IDE/ATA bus.

239. (New) The apparatus of claim 238, wherein said host interface is further operable to provide access by a microcontroller to data stored in locations addressed by at least certain of said ATA command block register addresses, said microcontroller operable to control reading of information from optical media.

240. (New) The apparatus of claim 238, wherein said optical drive controller further comprises:

a path operable to communicate said addresses and commands from the host interface to a microcontroller, said microcontroller operable to control reading of information from optical media.

241. The apparatus of claim 240, wherein said microcontroller is also operable to cause the assertion of signals on DASP and PDIAG lines of said IDE/ATA bus.

242. The apparatus of claim 240, wherein said microcontroller is also operable to cause the assertion of signals on an HIRQ line of said IDE/ATA bus to generate interrupts on said host computer.

243. The apparatus of claim 240, wherein:

said host interface includes a status register addressed by another of said ATA command block register addresses, said status register including a BSY bit whose state indicates whether said host computer can access said ATA command block register addresses; and

said microcontroller can cause said BSY bit to be altered to a state that allows access by said host computer.

244. (New) The apparatus of claim 238, wherein said ATA command block register addresses address eight register locations.

245. (New) The apparatus of claim 238, wherein said IDE/ATA bus includes,

host address lines; and

a host chip select line whose signal identifies whether signals on the host address lines are carrying one of said ATA command block register addresses.

246. (New) The apparatus of claim 238, wherein host interface includes physical registers that are addressed by at least certain of said ATA command block register addresses.

247. (New) The apparatus of claim 238, wherein said host interface supports all of the signals required by the ATA transfer protocol.

248. (New) The apparatus of claim 238, wherein said IDE/ATA bus is at least 16 bits wide.

249. (New) The apparatus of claim 238, wherein the one of said ATA command block register addresses that can be used to address said multi-byte command packet buffer is the address of a data port in the ATA transfer protocol.

250. (New) The apparatus of claim 238, wherein said host interface also includes a multi-byte data buffer operable to store data to be transmitted to said host computer and addressed by the one of said ATA command block register addresses that can be used to address said multi-byte command packet buffer.

251. (New) The apparatus of claim 250, wherein said multi-byte data buffer is a queue or FIFO.

252. (New) The apparatus of claim 238, wherein said multi-byte command packet buffer is a queue or FIFO.

253. (New) The apparatus of claim 238, wherein said optical drive controller further comprises:

a path operable to allow a microcontroller, which controls reading of information from optical media, to read said multi-byte command packet buffer.

254. (New) The apparatus of claim 238, wherein said host interface includes a status register addressed by another of said ATA command block register addresses, said status register including a BSY bit.

255. (New) The apparatus of claim 254, wherein said host interface alters said BSY bit when necessary to indicate when said host computer is precluded from accessing said ATA command block register addresses.

256. (New) The apparatus of claim 254, wherein said host interface includes circuitry operable to clear the signal on an HIRQ line of said IDE/ATA bus responsive to said host computer reading said status register.

257. (New) The apparatus of claim 254, wherein said host interface includes circuitry operable to alter said BSY bit, responsive to command events initiated by the host computer, to a state that precludes said host computer from accessing said ATA command block register addresses.

258. (New) The apparatus of claim 257, wherein said optical drive controller further comprises:

a path operable to allow a microcontroller, which controls reading of information from optical media, to alter said BSY bit to a state that allows said host computer to access said ATA command block register addresses.

259. (New) The apparatus of claim 257, wherein said host interface is operable to assert signals on DASP and PDIAG lines of said IDE/ATA bus according to the ATA transfer protocol.

260. (New) The apparatus of claim 259, wherein said host interface is also operable to assert signals on an HIRQ line of said IDE/ATA bus according to the ATA transfer protocol.

261. (New) The apparatus of claim 260, wherein said host interface includes circuitry operable to carry out initial signal transitions on said DASP, PDIAG, and HIRQ lines in response to soft reset and execute drive diagnostic command events.

262. (New) The apparatus of claim 261, wherein said optical drive controller further comprises:

a path operable to allow a microcontroller, which controls reading of information from optical media, to control certain transitions of signals on said DASP, PDIAG, and HIRQ lines of said IDE/ATA bus.

263. (New) The apparatus of claim 254, wherein said host interface is also operable to assert signals on DASP and PDIAG lines of said IDE/ATA bus responsive to power on reset or execute diagnostic commands received from said host computer.

264. (New) The apparatus of claim 263, wherein said optical drive controller further comprises:

a path operable to allow a microcontroller, which controls reading of information from optical media, to cause the assertion of signals on DASP and PDIAG lines of said IDE/ATA bus.

265. (New) The apparatus of claim 238, wherein said host interface includes a drive/head register addressed by another of said ATA command block register addresses, said drive/head register including a DRV bit.

266. (New) The apparatus of claim 265, wherein said host interface uses said DRV bit to determine whether to store command information in said multi-byte command packet buffer.

267. (New) The apparatus of claim 238, wherein said host interface is also operable to communicate control signals on at least certain control lines of said IDE/ATA bus.

268. (New) The apparatus of claim 267, wherein said control lines include HIRQ, DASP, and PDIAG.

269. (New) The apparatus of claim 238, wherein said host interface is also operable to assert signals on an HIRQ line of said IDE/ATA bus according to the ATA transfer protocol.

270. (New) The apparatus of claim 238, wherein said host interface is also operable to assert signals on an HIRQ line of said IDE/ATA bus to alert said host computer during data transfers.

271. (New) The apparatus of claim 238, wherein said host interface is also operable to assert signals on an HIRQ line of said IDE/ATA bus to allow said host computer to engage in multi-tasking.